| PTO-1449 (Modified)<br>U.S. DEPARTMENT OF COMMERCE<br>PATENT AND TRADEMARK OFFICE<br>INFORMATION DISCLOSURE STATEMENT BY APPLICANT | ATTY. DOCKET NO.<br>P043D2C2C | SERIAL NUMBER<br>09/252,997 |
|---|---|---|
| | APPLICANT(S)<br>FARMWALD ET AL. | |
| | FILING DATE<br>FEBRUARY 19, 1999 | GROUP ART UNIT<br>NOT ASSIGNED |

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|
| TNT | 4,445,204 | 04/24/84 | Nishiguchi | 365 | 194 | |
| | 4,821,226 | 04/11/89 | Christopher et al. | 365 | 230.08 | |
| | 4,882,712 | 11/21/89 | Ohno et. al. | 365 | 206 | |
| | 4,951,251 | 08/21/90 | Yamaguchi et al. | 365 | 189.02 | |
| | 4,928,265 | ~~12/29/92~~ 5 90 | Beighe et al. | 365 | 189.09 | |
| | 5,107,465 | 04/21/92 | Fung et al. | 365 | 230.08 | |
| | 5,206,833 | 04/27/93 | Lee | 365 | 233 | |
| TNT | 4,953,128 | 08/28/90 | Kawai et al. | 365 | 194 | |



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**FOREIGN PATENT DOCUMENTS**

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | |
|---|---|
| TNT | T.L. Jeremiah et. al., "SYNCHRONOUS PACKET SWITCHING MEMORY AND I/O CHANNEL," IBM Tech. Disc. Bul,. Vol. 24, No. 10, pp. 4986-4987 (Mar. 1982) |
| TNT | L. R. Metzeger, "A 16K CMOS PROM with Polysilicon Fusible Links", IEEE Journal of Solid State Circuits, vol. 18 No. 5, pp. 562-567 (Oct. 1983) |
| TNT | A. Yuen et. al., "A 32K ASIC Synchronous RAM Using a Two-Transistor Basic Cell", IEEE Journal of Solid State Circuits, vol. 24 No. 1, pp. 57-61 (Feb. 1989) |
| TNT | D.T. Wong et. al., "An 11-ns 8Kx18 CMOS Static RAM with 0.5-μm Devices", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1095-1103 (Oct. 1988) |
| TNT | T. Williams et. al., "An Experimental 1-Mbit CMOS SRAM with Configurable Organization and Operation", IEEE Journal of Solid State Circuits, vol. 23 No. 5, pp. 1085-1094 (Oct. 1988) |

| EXAMINER | Tan T. Nguyen | DATE CONSIDERED | 07/30/99 |
|---|---|---|---|

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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|---|---|---|
| | APPLICANT(S)<br>FARMWALD ET AL. | |
| | FILING DATE<br>FEBRUARY 19, 1999 | GROUP ART UNIT<br>NOT ASSIGNED |

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|
| TNT | 5,140,688 | 08/18/92 | White et al. | 395 | 550 | |
| | 5,018,111 | 05/21/91 | Madland | 365 | 233 | |
| | 4,734,880 | 03/29/88 | Collins | 711 | 105 | |
| | 4,183,095 | 01/08/80 | Ward | 365 | 189.02 | |
| | 4,975,872 | 12/04/90 | Zaiki | 365 | 49 | |
| | 5,016,226 | 05/14/91 | Hiwada et al. | 365 | 233 | |
| TNT | 5,109,498 | 04/28/92 | Kamiya et al. | 395 | 425 | |

**FOREIGN PATENT DOCUMENTS**

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | |
|---|---|
| TNT | D. Jones, "Synchronous static ram", Electronics and Wireless World, vol.93, no.1622, pp. 1243-4 (Dec. 87) |
| TNT | F. Miller et. al., "HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMS", Midcon/87 Conference Record, pp. 430-432 Chicago, IL, USA; 15-17 Sept. 1987 |
| TNT | K. Ohta, "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid State Circuits, vol. 21 No. 5, pp. 649-654 (Oct. 1986) |
| TNT | K. Nogami et. al., "A 9-ns HIT-Delay 32-kbyte Cache Macro for High-Speed RISC", IEEE Journal of Solid State Circuits, vol. 25 No. 1, pp. 100-108 (Feb. 1990) |
| TNT | F. Towler et. al., "A 128k 6.5ns Access/ 5ns Cycle CMOS ECL Static RAM", 1989 IEEE international Solid State Circuits Conference, (Feb. 1989) |
| TNT | M. Kimoto, "A 1.4ns/64kb RAM with 85ps/3680 Logic Gate Array", 1989 IEEE Custom Integrated Circuits Conference |

| EXAMINER | TANH T. NGUYEN | DATE CONSIDERED | 07/30/99 |
|---|---|---|---|

EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.

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|---|---|---|
| | APPLICANT(S)<br>FARMWALD ET AL. | |
| | FILING DATE<br>FEBRUARY 19, 1999 | GROUP ART UNIT<br>NOT ASSIGNED |

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUB CLASS | FILING DATE |
|---|---|---|---|---|---|---|
| TNT | 4,807,189 | 02/21/89 | Pinkham et al. | 365 | 189.05 | |
| | 4,092,665 | 05/30/78 | Saran | 341 | 63 | |
| | 4,799,199 | 01/17/89 | Scales, III et al. | 365 | 230.08 | |
| | 5,142,637 | 09/25/92 | Harlin et al. | 395 | 425 | |
| | 5,148,523 | 09/15/92 | Harlin et al. | 395 | 164 | |
| | 4,954,987 | 09/04/90 | Auvinen et al. | 365 | 189.02 | |
| | 4,675,850 | 06/23/87 | Nakano et al. | 365 | 230.01 | |
| | 4,788,667 | 05/22/90 | Higuchi | 365 | 193 | |
| | 4,937,734 | 06/26/90 | Bechtolsheim | 711 | 202 | |
| TNT | 4,680,738 | 07/14/87 | Tam | 365 | 239 | |

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FC pgms

**FOREIGN PATENT DOCUMENTS**

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUB CLASS | TRANSLATION YES/NO | |
|---|---|---|---|---|---|---|---|
| | | | | | | | |

**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | |
|---|---|
| TNT | D. Wendell et. al. "A 3.5ns, 2Kx9 Self Timed SRAM", 1990 IEEE Symposium on VLSI Circuits (Feb 1990) |
| TNT | M. Bazes et. al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, vol. 18 No. 2, pp. 164-172 (Apr. 1983) |
| TNT | R. Schmidt, "A memory Control Chip fo Formatting Data into Blocks Suitable for Video Applications", IEEE Transactions on Circuits and Systems, vol. 36, No. 10 (Oct. 1989) |
| TNT | D. K. Morgan "The CVAX CMCTL – A CMOS Memory Controller Chip", Digital Technical Journal, No. 7 (Aug. 1988) |
| TNT | T.C. Poon et. al., "A CMOS DRAM-Controller Chip Implementation", IEEE Journal of Solid State Circuits, vol. 22 No. 3, pp. 491-494 (June 1987) |
| TNT | K. Numata et. al. " New Nibbled-Page Architecture for High Density DRAM's", IEEE Journal of Solid State Circuits, vol. 24 No. 4, pp. 900-904 (Aug. 1989) |

| EXAMINER Tan T. Nguyen | DATE CONSIDERED 07/30/99 |
|---|---|

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